

# **Design and use of an array-based test structure to characterize mechanical stress effects caused by WLCSP solder bumps**

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## **Abstract**

This paper presents a DUT-array based test chip for characterizing mechanical stress effects attributable to Wafer Level Chip Scale Package solder bumps. Detailed DUT cell layout requirements, array implementation, measurement approach, and some data analysis challenges are discussed and illustrated with several unique solder bump induced mobility variation examples.

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**Oral** presentation preferred

# Design and use of an array-based test structure to characterize mechanical stress effects caused by WLCSP solder bumps

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**Introduction.** Wafer Level Chip Scale Packaging (WLCSP) implies direct soldering of silicon dies onto printed circuit boards. Due to thermal expansion coefficient differences of chip, solder ball (Fig. 1a) and PCB, WLCSP inflicts mechanical stress on circuit components below or near solder bumps. The impact of bump-attributable *sub-1%* device variations on yield of electronically trimmed circuit blocks will be presented in [1]. To support this work we designed a dedicated high precision array-based test structure that combines high measurement accuracy (<0.1%) with very good (10  $\mu\text{m}$ ) spatial resolution. The design obviously leans heavily on learnings from prior art CMOS multiplexer-based test chips [2-9]. Results were used to verify and calibrate the methodology introduced in [1]. In this proposed ICMTS paper we will discuss details of DUT cell design and required measurement and analysis techniques, illustrated with some bump stress effects obtained with these 2100-DUT arrays.

**Test Structure.** Fig. 1 shows the test chip layout and an example of a test die featuring an array of 70 x 30 identical devices below two ( $\approx 200 \mu\text{m}$  diameter) bumps. Each of the 2100 devices of the array is Force-Sense accessible through switches in the DUT cell and a shift-register based cell selection (Fig. 2). The DUT, e.g. a P-active resistor in Fig. 2a, is folded to maximize its resistance relative to the addressing and pad protection circuitry. The DUT cell (pitch  $10 \times 10 \mu\text{m}^2$ ; DUT area  $\approx 20 \mu\text{m}^2$ ) results from the trade-off between reachable measurement accuracy and spatial resolution: a smaller pitch gives better spatial resolution, but the smaller DUT (larger random fluctuations) decreases the measurable resistance change resolution. Density layout rules of the used 7-metal 90 nm CMOS foundry technology also limit the usable DUT area within a DUT cell. Access transistors were minimized to create space for dummies in the cell to meet density requirements. Lower-metal tiling was avoided on the DUTs. Array wiring was optimized to provide identical total interconnect lengths to each DUT. The WLCSP bumps on the array are grounded to prevent EMC disturbances. D-flipflops, buffers of the shift register and access transistors in the DUT cells are GO2 MOSTs, chosen for their larger voltage span. MOSFET DUTs are tied gate-to-drain inside the DUT cell. For BJTs the SMUs are connected to Base and Emitter, and Collector is grounded.

**Measurement approach.** The arrays are measured on-wafer using a C-M 12k prober with eight coaxial W needles probing on SnAg solder balls. Measurements were done using an HP4156B SPA controlled through Flex commands from a LabVIEW program. The four SMUs drive the two DUT Force terminals, and VDD and GND. The VMUs sense the DUT voltages and the VSUs provide clocking and address input. A 100 bit word is clocked into the shift register for each DUT through hi-lo switching of the VSUs. All measurements are done with medium integration at typical DUT currents ranging from 0.1 to 50  $\mu\text{A}$ . Measuring a 2100-DUT array typically takes 50 minutes, dominated by the 100-bit-word clocking. The measurement repeatability (< 0.02%) is well within the requirements. Resistor DUTs are biased below 0.2 V for maximum measurement resolution in the differential voltage measurement mode of the VMUs. The total resistance in the force paths (pads, protection circuitry, interconnect, switches) is about 2 k $\Omega$ . The leakage current at the internal DUT nodes was estimated at less than 100 pA. The usable DUT current range for this type of DUT arrays hence range from about 10 nA to 100  $\mu\text{A}$ .

**Results.** Typical examples of results obtained with the 2100-DUT arrays are depicted in Figures 3 to 6. They clearly demonstrate effects of bumps on the mobility of different device types. Although the actual DUTs are already relatively large, averaging over 10 arrays is used to mitigate random variations (Fig. 3). For purposes demanding more precision (e.g. modeling), averaging over multiple columns through the center of the bumps is used (Fig 6 c). Arrays suffering from parametric gradients that are not caused by the solder bumps are corrected using linear plane fitting (Fig. 4). Figures 5 and 6 give flavors of some of the fascinating conclusions that were drawn using these bump stress test arrays. For the first time we created a comprehensive overview of the impact of WLCSP solder balls on the mobility of all major IC components (Fig. 5). Clear differences as well as similarities in direction, magnitude, and sensitivity to construction features are observed amongst different device types. These observations were used to fine-tune Piezo coefficients required for the methodology reported in [1]. In the VPNP arrays (Fig. 6) we found that not only the bumps but also the (tensile) stress from the Alu-pad layer affects the current. The “blue spectacles” in Fig. 6b represent an average current reduction by about 0.3%. Moreover, Fig. 6c reveals that  $\sigma_{\Delta I_c/I_c}$  increases from 0.05% outside the bump to 0.15% under the center of the bump, confirming (suspected) random crystallization and stress relaxation effects during solidification of the molten bumps.

**Conclusion.** Results obtained using 2100-DUT array test structures and the associated analysis techniques demonstrate an outstanding bump stress characterization resolution. These test structures consequently provide unique and valuable insight in the impact of WLCSP solder bumps on circuit devices placed under or near these bumps.

## References

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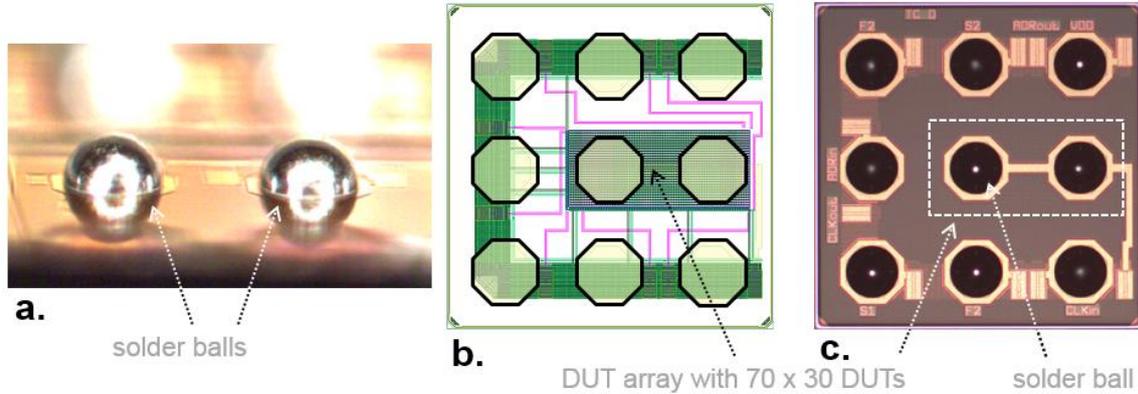


Fig. 1. *a:* plated WLCSP solder balls on the test chip. *b:* layout with 2100-DUT array placed under two WLCSP pads. *c:* Test chip photograph with solder balls on the eight measurement pads: VDD, GND, Forces, Senses, Click\_in, Addr\_in. The ball in the center of the die is not probed but tied to ground using the Alu-pad interconnect layer. These solder balls have a diameter of about 200  $\mu$ m.

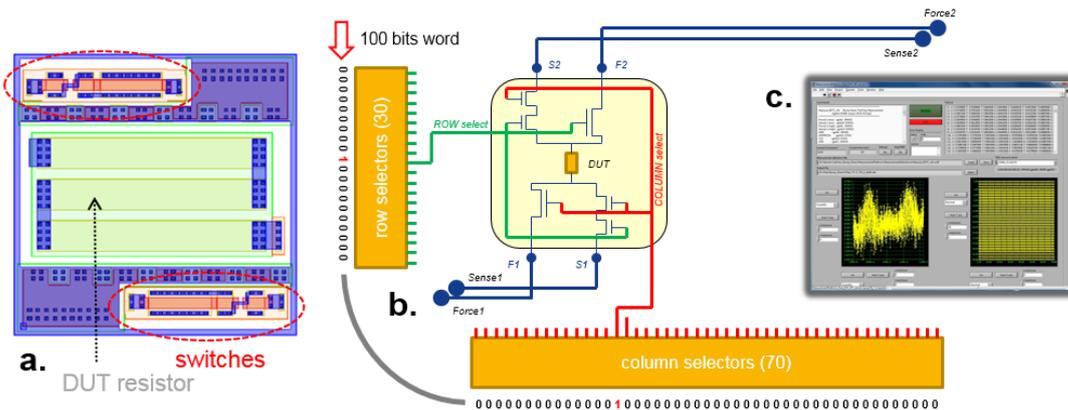


Fig. 2. Force - Sense measurement approach of 2100 DUTs. *a:* Example of layout of DUT cell (up to Metal-1) with folded DUT (in this case a P-active resistor) and six access transistors (switches). *b:* DUT selection through a 30+70 stage shift register, addressed using a 100 bit word. *c:* GUI of LabVIEW program that drives an HP4156B semiconductor parameter analyzer.

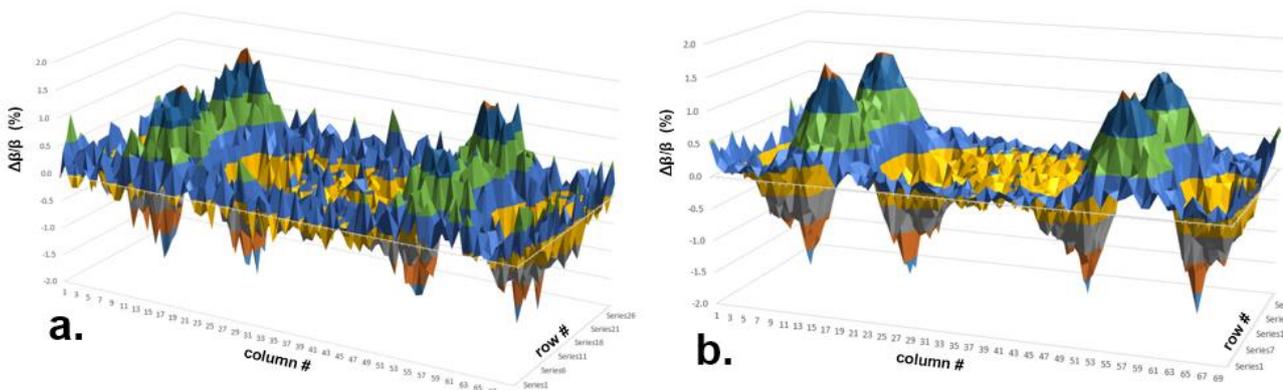


Fig. 3. Example of (relative) transconductance variations in 2100-DUT arrays for PMOS transistors. *a:* the pattern from one array is naturally noisy due to random mismatch fluctuations ( $\sigma_{\Delta\beta/\beta}$  typ. 0.2 to 0.25 %). *b:* average of ten arrays reduces random fluctuations by factor  $\sqrt{10}$ . Mobility (transconductance) variability patterns and position and effects of bumps are now clearly distinguishable and usable for modeling purposes.

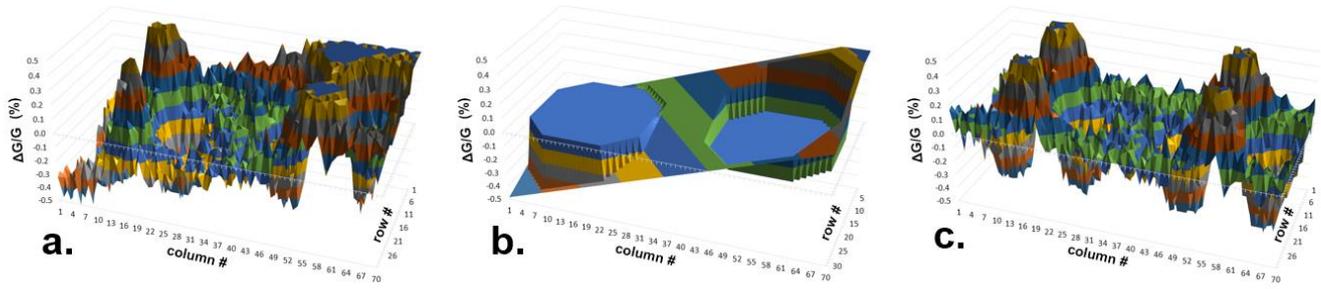


Fig. 4. Example of (relative) conductance variability in a 2100-DUT array for P-active resistors.  
**a:** 3-D plot of raw data for 2100 DUTs shows clear systematic gradient across the array.  
**b:** fitting plane to correct for array gradient.  
**c:** Flattened pattern still somewhat noisy due to random resistor mismatch fluctuations (1 array).

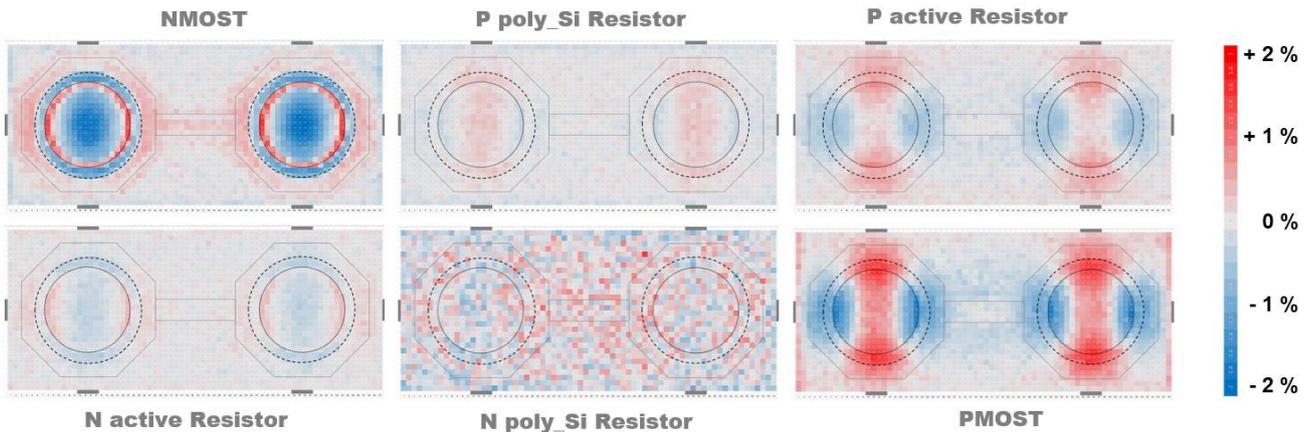


Fig. 5 Overview of measured (trans-) conductance variation patterns for different types of DUT arrays (averaged over 10 arrays each).  
 Directional differences are attributable to angle of mechanical stress vector and current flow direction (“East-West”).  
 Note similarity of patterns for all P-type DUTs and idem for N-active resistors and NMOSTs.  
 Also note distinct effects of WLCSP layers and mask edges, particularly for NMOSTs.  
 WLCSP process and mask features superimposed on maps: Dotted octagons = top metal (Alu Pad see also Fig. 1c);  
 Bold dashed circles = Under Bump Metal; fine dashed circles = Poly-Imide isolation openings.  
 Random fluctuations dominate over stress effects in N-type poly resistor arrays (lower center).

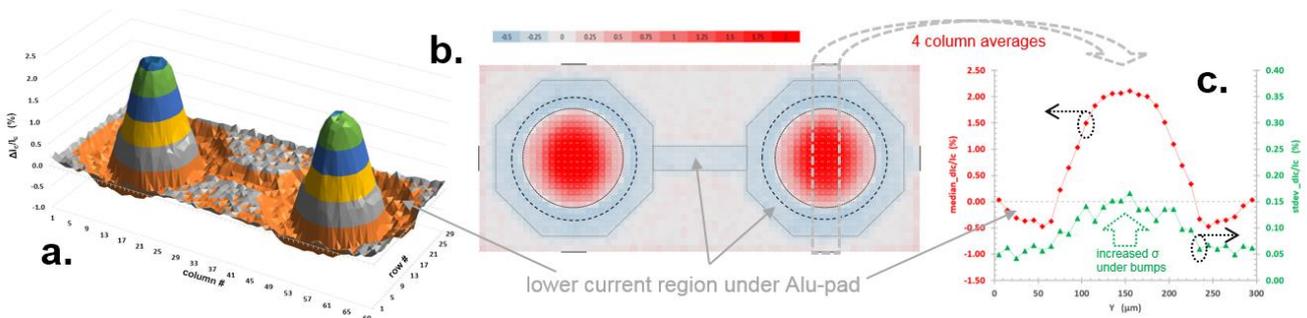


Fig. 6. Measurement results of collector current variations for vertical PNP BJT 2100-DUT arrays demonstrating some subtle and fascinating effects of WLCSP solder bump processing.

**a:** 3-D plot of 2100-DUT array with two bumps, **b:** color-scale plot of same data.  
 Note that Alu-pad metallization reduces current by almost 0.5 % (“blue spectacles” in **b.** & “orange trenches” in **a.**).  
**c:** cross-section in vertical direction through bump (median and standard deviation based on 30 bumps & 4 column averages).  
 Standard deviation of collector current variability (green triangles in right figure) increases from 0.05% outside of bump to 0.15% in the middle of the bump, suggesting dominant variability due to solder crystallization and stress relaxation.  
 Data (also) averaged from 4 (very similar) columns through the center of the bump.

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